WHAT IS CLAIMED IS:

1. A video decoding device for decoding a coded video signal which is supplied to the video decoding device as packets each of which containing a plurality of coded block data units which have been generated by encoding blocks each of which is composed of a predetermined number of pixels of a frame of a video signal, comprising:

an error detection means for judging whether or not an error has occurred to each of the packets and outputting a judgment signal indicating the result of the judgment;

a packet partitioning means for partitioning the packet after the error detection by the error detection means into the coded block data units, while outputting an address signal indicating addresses of blocks that have been contained in the packets to which the errors have occurred;

a video decoding means for successively decoding the coded block data units and outputting a decoded video signal containing block data units obtained by the decoding of the coded block data units;

a first invalid block judgment means for judging whether or not each of the block data units corresponding to the addresses indicated by the address signal from the packet partitioning means is an invalid block which has been decoded abnormally, based on pixel values of adjacent blocks; and

a first invalid block concealment means for conducting a concealment process with regard to the block data units that have been judged by the first invalid block judgment means as invalid blocks.

2. A video decoding device as claimed in claim 1, wherein the error detection means conducts the judgment for each packet by use of error detection code which has been contained in the packet.

3. A video decoding device as claimed in claim 1, wherein the first invalid block judgment means includes:

a judgment value calculation means for calculating a judgment value concerning pixel value variation with regard to each pixel in the block designated by the address signal from the packet partitioning means, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison means for successively comparing the judgment value with regard to each pixel calculated by the judgment value calculation means with a first threshold value and successively outputting a comparison result signal with regard to each pixel;

a flag storage means for storing a flag which is incremented depending on the comparison result signal with regard to each pixel; and

a second comparison means for comparing the value of the flag with a second threshold value.

4. A video decoding device as claimed in claim 1, wherein the first invalid block concealment means conducts the concealment process by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

5. A video decoding device as claimed in claim 1, wherein the first invalid block concealment means conducts the concealment process by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame.

6. A video decoding device as claimed in claim 1, wherein the video decoding device is applied to cases where the packets are TCP

(Transmission Control Protocol) packets, UDP (User Datagram Protocol) packets or ATM (Asynchronous Transfer Mode) cells.

7. A video decoding device as claimed in claim 1, wherein the video decoding means includes:

a frame memory means for storing the block data units of previously decoded frames and the block data units of a currently decoded frame;

a block data decoding means for successively decoding the coded block data units and outputting the block data units obtained by the decoding of the coded block data units, while outputting an address signal indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data; and

a second invalid block concealment means for conducting a concealment process with regard to the block data units corresponding to the addresses indicated by the address signal from the block data decoding means.

8. A video decoding device as claimed in claim 7, wherein the block data decoding means conducts the decoding of the coded block data units by use of block data units of the previous frame which have been stored in the frame memory means.

9. A video decoding device as claimed in claim 7, wherein the second invalid block concealment means conducts the concealment process by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

10. A video decoding device as claimed in claim 7, wherein the

second invalid block concealment means conducts the concealment process by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame.

11. A video decoding device as claimed in claim 1, wherein the video decoding means includes:

a frame memory means for storing the block data units of previously decoded frames and the block data units of a currently decoded frame;

a block data decoding means for successively decoding the coded block data units and outputting the block data units obtained by the decoding of the coded block data units, while outputting an address signal indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data;

a second invalid block concealment means for conducting a concealment process with regard to the block data units corresponding to the addresses indicated by the address signal from the block data decoding means;

a second invalid block judgment means for judging whether or not each block data unit obtained by the concealment process of the second invalid block concealment means is an invalid block whose pixel values are inadequate, based on pixel values of adjacent blocks; and

a third invalid block concealment means for conducting a concealment process with regard to the block data units which have been judged by the second invalid block judgment means as invalid blocks.

12. A video decoding device as claimed in claim 11, wherein the block data decoding means conducts the decoding of the coded block data units by use of block data units of the previous frame which have been

stored in the frame memory means.

13. A video decoding device as claimed in claim 11, wherein the second invalid block judgment means includes:

a judgment value calculation means for calculating a judgment value concerning pixel value variation with regard to each pixel in the block designated by the address signal from the packet partitioning means, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison means for successively comparing the judgment value with regard to each pixel calculated by the judgment value calculation means with a first threshold value and successively outputting a comparison result signal with regard to each pixel;

a flag storage means for storing a flag which is incremented depending on the comparison result signal with regard to each pixel; and

a second comparison means for comparing the value of the flag with a second threshold value.

14. A video decoding device as claimed in claim 11, wherein:

the second invalid block concealment means conducts the concealment process by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame, and

the third invalid block concealment means conducts the concealment process by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

15. A video decoding device for decoding a coded video signal which is supplied to the video decoding device as packets each of which

containing a plurality of coded block data units which have been generated by encoding blocks each of which is composed of a predetermined number of pixels of a frame of a video signal, comprising:

an error detection means for judging whether or not an error has occurred to each of the packets and outputting a judgment signal indicating the result of the judgment;

a packet partitioning means for partitioning the packet after the error detection by the error detection means into the coded block data units, while outputting an address signal indicating addresses of blocks that have been contained in the packets to which the errors have occurred; and

a video decoding means for successively decoding the coded block data units and outputting a decoded video signal containing block data units obtained by the decoding of the coded block data units, which includes:

a frame memory means for storing the block data units of previously decoded frames and the block data units of a currently decoded frame;

a block data decoding means for successively decoding the coded block data units and outputting the block data units obtained by the decoding of the coded block data units, while outputting an address signal indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data;

a second invalid block concealment means for conducting a concealment process with regard to the block data units corresponding to the addresses indicated by the address signal from the block data decoding means;

a second invalid block judgment means for judging whether or not each block data unit obtained by the concealment process of the second invalid block concealment means is an invalid block whose pixel

values are inadequate, based on pixel values of adjacent blocks; and

a third invalid block concealment means for conducting a concealment process with regard to the block data units which have been judged by the second invalid block judgment means as invalid blocks.

16. A video decoding device as claimed in claim 15, wherein the error detection means conducts the judgment for each packet by use of error detection code which has been contained in the packet.

17. A video decoding device as claimed in claim 15, wherein the block data decoding means conducts the decoding of the coded block data units by use of block data units of the previous frame which have been stored in the frame memory means.

18. A video decoding device as claimed in claim 15, wherein the second invalid block judgment means includes:

a judgment value calculation means for calculating a judgment value concerning pixel value variation with regard to each pixel in the block designated by the address signal from the packet partitioning means, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison means for successively comparing the judgment value with regard to each pixel calculated by the judgment value calculation means with a first threshold value and successively outputting a comparison result signal with regard to each pixel;

a flag storage means for storing a flag which is incremented depending on the comparison result signal with regard to each pixel; and

a second comparison means for comparing the value of the flag with a second threshold value.

19. A video decoding device as claimed in claim 15, wherein:

the second invalid block concealment means conducts the concealment process by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame, and

the third invalid block concealment means conducts the concealment process by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

20. A video decoding device as claimed in claim 15, wherein the video decoding device is applied to cases where the packets are TCP (Transmission Control Protocol) packets, UDP (User Datagram Protocol) packets or ATM (Asynchronous Transfer Mode) cells.

21. A video decoding method for decoding a coded video signal which is supplied as packets each of which containing a plurality of coded block data units which have been generated by encoding blocks each of which is composed of a predetermined number of pixels of a frame of a video signal, comprising the steps of:

an error detection step in which whether or not an error has occurred to each of the packets is judged and a judgment signal indicating the result of the judgment is generated;

a packet partitioning step in which the packet after the error detection of the error detection step is partitioned into the coded block data units, while an address signal, indicating addresses of blocks that have been contained in the packets to which the errors have occurred, is generated;

a video decoding step in which the coded block data units are successively decoded in order to generate a decoded video signal

containing block data units obtained by the decoding of the coded block data units;

a first invalid block judgment step in which it is judged whether or not each of the block data units corresponding to the addresses indicated by the address signal generated in the packet partitioning step is an invalid block which has been decoded abnormally, based on pixel values of adjacent blocks; and

a first invalid block concealment step in which a concealment process is conducted for the block data units that have been judged in the first invalid block judgment step as invalid blocks.

22. A video decoding method as claimed in claim 21, wherein in the error detection step, the judgment for each packet is conducted by use of error detection code which has been contained in the packet.

23. A video decoding method as claimed in claim 21, wherein the first invalid block judgment step includes:

a judgment value calculation step in which a judgment value concerning pixel value variation is calculated with regard to each pixel in the block designated by the address signal generated in the packet partitioning step, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison step in which the judgment value with regard to each pixel calculated in the judgment value calculation step is successively compared with a first threshold value and a comparison result signal with regard to each pixel is successively generated;

a flag increment step in which a flag which is stored in a flag storage means is successively incremented depending on the comparison result signal with regard to each pixel; and

a second comparison step in which the value of the flag is

compared with a second threshold value.

24. A video decoding method as claimed in claim 21, wherein in the first invalid block concealment step, the concealment process is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

25. A video decoding method as claimed in claim 21, wherein in the first invalid block concealment step, the concealment process is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame.

26. A video decoding method as claimed in claim 21, wherein the video decoding method is applied to cases where the packets are TCP (Transmission Control Protocol) packets, UDP (User Datagram Protocol) packets or ATM (Asynchronous Transfer Mode) cells.

27. A video decoding method as claimed in claim 21, wherein the video decoding step includes:

a frame memory storage step in which the block data units of previously decoded frames and the block data units of a currently decoded frame are stored in a frame memory means;

a block data decoding step in which the coded block data units are successively decoded and thereby the block data units as the result of the decoding are obtained, while an address signal, indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data, is generated; and

a second invalid block concealment step in which a concealment

process is conducted for the block data units corresponding to the addresses indicated by the address signal generated in the block data decoding step.

28. A video decoding method as claimed in claim 27, wherein in the block data decoding step, the decoding of the coded block data units is conducted by use of block data units of the previous frame which have been stored in the frame memory means.

29. A video decoding method as claimed in claim 27, wherein in the second invalid block concealment step, the concealment process is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

30. A video decoding method as claimed in claim 27, wherein in the second invalid block concealment step, the concealment process is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame.

31. A video decoding method as claimed in claim 21, wherein the video decoding step includes:

a frame memory storage step in which the block data units of previously decoded frames and the block data units of a currently decoded frame are stored in a frame memory means;

a block data decoding step in which the coded block data units are successively decoded and thereby the block data units as the result of the decoding are obtained, while an address signal, indicating addresses of blocks which could not be decoded normally due to errors contained in the

coded block data, is generated;

a second invalid block concealment step in which a concealment process is conducted for the block data units corresponding to the addresses indicated by the address signal generated in the block data decoding step;

a second invalid block judgment step in which it is judged whether or not each block data unit obtained by the concealment process in the second invalid block concealment step is an invalid block whose pixel values are inadequate, based on pixel values of adjacent blocks; and

a third invalid block concealment step in which a concealment process is conducted for the block data units which have been judged in the second invalid block judgment step as invalid blocks.

32. A video decoding method as claimed in claim 31, wherein in the block data decoding step, the decoding of the coded block data units is conducted by use of block data units of the previous frame which have been stored in the frame memory means.

33. A video decoding method as claimed in claim 31, wherein the second invalid block judgment step includes:

a judgment value calculation step in which a judgment value concerning pixel value variation is calculated with regard to each pixel in the block designated by the address signal generated in the packet partitioning step, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison step in which the judgment value with regard to each pixel calculated in the judgment value calculation step is successively compared with a first threshold value and a comparison result signal with regard to each pixel is successively generated;

a flag increment step in which a flag which is stored in a flag

storage means is successively incremented depending on the comparison result signal with regard to each pixel; and

a second comparison step in which the value of the flag is compared with a second threshold value.

34. A video decoding method as claimed in claim 31, wherein:

the concealment process in the second invalid block concealment step is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame, and

the concealment process in the third invalid block concealment step is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

35. A video decoding method for decoding a coded video signal which is supplied as packets each of which containing a plurality of coded block data units which have been generated by encoding blocks each of which is composed of a predetermined number of pixels of a frame of a video signal, comprising the steps of:

an error detection step in which whether or not an error has occurred to each of the packets is judged and a judgment signal indicating the result of the judgment is generated;

a packet partitioning step in which the packet after the error detection of the error detection step is partitioned into the coded block data units, while an address signal, indicating addresses of blocks that have been contained in the packets to which the errors have occurred, is generated; and

a video decoding step in which the coded block data units are successively decoded in order to generate a decoded video signal

containing block data units obtained by the decoding of the coded block data units, which includes:

a frame memory storage step in which the block data units of previously decoded frames and the block data units of a currently decoded frame are stored in a frame memory means;

a block data decoding step in which the coded block data units are successively decoded and thereby the block data units as the result of the decoding are obtained, while an address signal, indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data, is generated;

a second invalid block concealment step in which a concealment process is conducted for the block data units corresponding to the addresses indicated by the address signal generated in the block data decoding step;

a second invalid block judgment step in which it is judged whether or not each block data unit obtained by the concealment process in the second invalid block concealment step is an invalid block whose pixel values are inadequate, based on pixel values of adjacent blocks; and

a third invalid block concealment step in which a concealment process is conducted for the block data units which have been judged in the second invalid block judgment step as invalid blocks.

36. A video decoding method as claimed in claim 35, wherein in the error detection step, the judgment for each packet is conducted by use of error detection code which has been contained in the packet.

37. A video decoding method as claimed in claim 35, wherein in the block data decoding step, the decoding of the coded block data units is conducted by use of block data units of the previous frame which have been stored in the frame memory means.

38. A video decoding method as claimed in claim 35, wherein the second invalid block judgment step includes:

a judgment value calculation step in which a judgment value concerning pixel value variation is calculated with regard to each pixel in the block designated by the address signal generated in the packet partitioning step, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison step in which the judgment value with regard to each pixel calculated in the judgment value calculation step is successively compared with a first threshold value and a comparison result signal with regard to each pixel is successively generated;

a flag increment step in which a flag which is stored in a flag storage means is successively incremented depending on the comparison result signal with regard to each pixel; and

a second comparison step in which the value of the flag is compared with a second threshold value.

39. A video decoding method as claimed in claim 35, wherein:

the concealment process in the second invalid block concealment step is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame, and

the concealment process in the third invalid block concealment step is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

40. A video decoding method as claimed in claim 35, wherein the video decoding method is applied to cases where the packets are TCP (Transmission Control Protocol) packets, UDP (User Datagram Protocol)

packets or ATM (Asynchronous Transfer Mode) cells.

41. A machine-readable record medium storing a program for instructing an MPU (MicroProcessor Unit) etc. to execute a video decoding process for decoding a coded video signal which is supplied as packets each of which containing a plurality of coded block data units which have been generated by encoding blocks each of which is composed of a predetermined number of pixels of a frame of a video signal, wherein the video decoding process comprises the steps of:

an error detection step in which whether or not an error has occurred to each of the packets is judged and a judgment signal indicating the result of the judgment is generated;

a packet partitioning step in which the packet after the error detection of the error detection step is partitioned into the coded block data units, while an address signal, indicating addresses of blocks that have been contained in the packets to which the errors have occurred, is generated;

a video decoding step in which the coded block data units are successively decoded in order to generate a decoded video signal containing block data units obtained by the decoding of the coded block data units;

a first invalid block judgment step in which it is judged whether or not each of the block data units corresponding to the addresses indicated by the address signal generated in the packet partitioning step is an invalid block which has been decoded abnormally, based on pixel values of adjacent blocks; and

a first invalid block concealment step in which a concealment process is conducted for the block data units that have been judged in the first invalid block judgment step as invalid blocks.

42. A machine-readable record medium as claimed in claim 41, wherein in the error detection step, the judgment for each packet is conducted by use of error detection code which has been contained in the packet.

43. A machine-readable record medium as claimed in claim 41, wherein the first invalid block judgment step includes:

a judgment value calculation step in which a judgment value concerning pixel value variation is calculated with regard to each pixel in the block designated by the address signal generated in the packet partitioning step, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison step in which the judgment value with regard to each pixel calculated in the judgment value calculation step is successively compared with a first threshold value and a comparison result signal with regard to each pixel is successively generated;

a flag increment step in which a flag which is stored in a flag storage means is successively incremented depending on the comparison result signal with regard to each pixel; and

a second comparison step in which the value of the flag is compared with a second threshold value.

44. A machine-readable record medium as claimed in claim 41, wherein in the first invalid block concealment step, the concealment process is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

45. A machine-readable record medium as claimed in claim 41, wherein in the first invalid block concealment step, the concealment

process is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame.

46. A machine-readable record medium as claimed in claim 41, wherein the video decoding process is applied to cases where the packets are TCP (Transmission Control Protocol) packets, UDP (User Datagram Protocol) packets or ATM (Asynchronous Transfer Mode) cells.

47. A machine-readable record medium as claimed in claim 41, wherein the video decoding step includes:

a frame memory storage step in which the block data units of previously decoded frames and the block data units of a currently decoded frame are stored in a frame memory means;

a block data decoding step in which the coded block data units are successively decoded and thereby the block data units as the result of the decoding are obtained, while an address signal, indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data, is generated; and

a second invalid block concealment step in which a concealment process is conducted for the block data units corresponding to the addresses indicated by the address signal generated in the block data decoding step.

48. A machine-readable record medium as claimed in claim 47, wherein in the block data decoding step, the decoding of the coded block data units is conducted by use of block data units of the previous frame which have been stored in the frame memory means.

49. A machine-readable record medium as claimed in claim 47,

wherein in the second invalid block concealment step, the concealment process is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

50. A machine-readable record medium as claimed in claim 47, wherein in the second invalid block concealment step, the concealment process is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame.

51. A machine-readable record medium as claimed in claim 41, wherein the video decoding step includes:

a frame memory storage step in which the block data units of previously decoded frames and the block data units of a currently decoded frame are stored in a frame memory means;

a block data decoding step in which the coded block data units are successively decoded and thereby the block data units as the result of the decoding are obtained, while an address signal, indicating addresses of blocks which could not be decoded normally due to errors contained in the coded block data, is generated;

a second invalid block concealment step in which a concealment process is conducted for the block data units corresponding to the addresses indicated by the address signal generated in the block data decoding step;

a second invalid block judgment step in which it is judged whether or not each block data unit obtained by the concealment process in the second invalid block concealment step is an invalid block whose pixel values are inadequate, based on pixel values of adjacent blocks; and

a third invalid block concealment step in which a concealment

process is conducted for the block data units which have been judged in the second invalid block judgment step as invalid blocks.

52. A machine-readable record medium as claimed in claim 51, wherein in the block data decoding step, the decoding of the coded block data units is conducted by use of block data units of the previous frame which have been stored in the frame memory means.

53. A machine-readable record medium as claimed in claim 51, wherein the second invalid block judgment step includes:

a judgment value calculation step in which a judgment value concerning pixel value variation is calculated with regard to each pixel in the block designated by the address signal generated in the packet partitioning step, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison step in which the judgment value with regard to each pixel calculated in the judgment value calculation step is successively compared with a first threshold value and a comparison result signal with regard to each pixel is successively generated;

a flag increment step in which a flag which is stored in a flag storage means is successively incremented depending on the comparison result signal with regard to each pixel; and

a second comparison step in which the value of the flag is compared with a second threshold value.

54. A machine-readable record medium as claimed in claim 51, wherein:

the concealment process in the second invalid block concealment step is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values

of an appropriate block data unit of the previous frame, and

the concealment process in the third invalid block concealment step is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

55. A machine-readable record medium for decoding a coded video signal which is supplied as packets each of which containing a plurality of coded block data units which have been generated by encoding blocks each of which is composed of a predetermined number of pixels of a frame of a video signal, comprising the steps of:

an error detection step in which whether or not an error has occurred to each of the packets is judged and a judgment signal indicating the result of the judgment is generated;

a packet partitioning step in which the packet after the error detection of the error detection step is partitioned into the coded block data units, while an address signal, indicating addresses of blocks that have been contained in the packets to which the errors have occurred, is generated; and

a video decoding step in which the coded block data units are successively decoded in order to generate a decoded video signal containing block data units obtained by the decoding of the coded block data units, which includes:

a frame memory storage step in which the block data units of previously decoded frames and the block data units of a currently decoded frame are stored in a frame memory means;

a block data decoding step in which the coded block data units are successively decoded and thereby the block data units as the result of the decoding are obtained, while an address signal, indicating addresses of blocks which could not be decoded normally due to errors

contained in the coded block data, is generated;

a second invalid block concealment step in which a concealment process is conducted for the block data units corresponding to the addresses indicated by the address signal generated in the block data decoding step;

a second invalid block judgment step in which it is judged whether or not each block data unit obtained by the concealment process in the second invalid block concealment step is an invalid block whose pixel values are inadequate, based on pixel values of adjacent blocks; and

a third invalid block concealment step in which a concealment process is conducted for the block data units which have been judged in the second invalid block judgment step as invalid blocks.

56. A machine-readable record medium as claimed in claim 55, wherein in the error detection step, the judgment for each packet is conducted by use of error detection code which has been contained in the packet.

57. A machine-readable record medium as claimed in claim 55, wherein in the block data decoding step, the decoding of the coded block data units is conducted by use of block data units of the previous frame which have been stored in the frame memory means.

58. A machine-readable record medium as claimed in claim 55, wherein the second invalid block judgment step includes:

a judgment value calculation step in which a judgment value concerning pixel value variation is calculated with regard to each pixel in the block designated by the address signal generated in the packet partitioning step, by referring to pixel values of the designated block and/or pixel values of adjacent blocks;

a first comparison step in which the judgment value with regard to each pixel calculated in the judgment value calculation step is successively compared with a first threshold value and a comparison result signal with regard to each pixel is successively generated;

a flag increment step in which a flag which is stored in a flag storage means is successively incremented depending on the comparison result signal with regard to each pixel; and

a second comparison step in which the value of the flag is compared with a second threshold value.

59. A machine-readable record medium as claimed in claim 55, wherein:

the concealment process in the second invalid block concealment step is conducted by means of an inter-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of an appropriate block data unit of the previous frame, and

the concealment process in the third invalid block concealment step is conducted by means of an intra-frame concealment process in which pixel values of the block data unit is corrected by use of pixel values of adjacent blocks in the current frame.

60. A machine-readable record medium as claimed in claim 55, wherein the video decoding process is applied to cases where the packets are TCP (Transmission Control Protocol) packets, UDP (User Datagram Protocol) packets or ATM (Asynchronous Transfer Mode) cells.